overview

- within flash block, when one page is read, \( V_{pass} \) (pass-through voltage) applied to other pages.
- pass-through voltage has a weak programming effect – in unread pages, stored voltages increase over time: read disturb.
- characterize impact of read disturb errors on real 2Y-nm flash chips.
- two solutions for read disturb:
  - mitigation by performing dynamic \( V_{pass} \) tuning
  - recovery by reversing read disturb behavior.

read disturb mitigation: \( V_{pass} \) tuning

- lowering \( V_{pass} \) reduces read disturb errors, but can introduce new read errors – improper pass-through.
- exploit unused ECC capability to correct the new errors.
- dynamically tune \( V_{pass} \) to maximize unused ECC.
- avg. lifetime increase on real-world apps: 21%.

overhead

- hw: 2 bytes per block (128 KB for 512 GB SSD)
- performance: 24.34 sec/day.

read disturb oriented error recovery

- some flash cells more susceptible to read disturb.
  - disturb-prone cells (P): large voltage shifts to high end of state distribution.
  - disturb-resistant cells (R): small shifts, remaining in low end of distribution.
- example: voltage shifts after 250K read disturbs.

- state boundary shifts: cells now incorrectly read.
- once flash lifetime ends (too many errors for ECC), recover data by reversing read disturb.
  - induce more read disturbs to ID prone/resistant.
  - predict prone cells \( \rightarrow \) lower state.
  - predict resistant cells \( \rightarrow \) higher state.
  - ECC handles remaining corrections.
- after 1M read disturbs, recovery can reduce error count by 36%.